Machine translation JP2001177401

(19)**Publication country**Japan Patent Office (JP)
(12)**Kind of official gazette**Publication of patent applications (A)
(11)**Publication No.**JP,2001-177401,A (P2001-177401A)
(43)**Date of Publication**Heisei 13(2001) June 29 (2001.6.29)
(54)**Title of the Invention**Phase synchronization circuit
(51)**The 7th edition of International Patent Classification**

H03L 7/095

7/093

7/08

H04L 7/033
FI

H03L 7/08 B

E

M

H04L 7/02 B
Request for Examination Unrequested
The number of claims 11
Mode of ApplicationOL
Number of Pages14
(21)**Application number**Japanese Patent Application No. 11-359158
(22)**Filing date**Heisei 11(1999) December 17 (1999.12.17)
(71)**Applicant**
Identification Number000006013
NameMITSUBISHI DENKI KABUSHIKI KAISHA
Address2-2-3, Marunouchi, Chiyoda-ku, Tokyo
(72)**Inventor(s)**
NameAkio Sasai
Address2-6-2, Otemachi, Chiyoda-ku, Tokyo Inside of MITSUBISHI ELECTRIC ENGINEERING COMPANY LIMITED
(72)**Inventor(s)**
NameKosaka Intelligent
Address2-2-3, Marunouchi, Chiyoda-ku, Tokyo Inside of MITSUBISHI DENKI KABUSHIKI KAISHA
(74)**Attorney**
Identification Number100102439
Patent Attorney
NameMIYATA, Kaneo (and 1 others)
Theme code (reference)

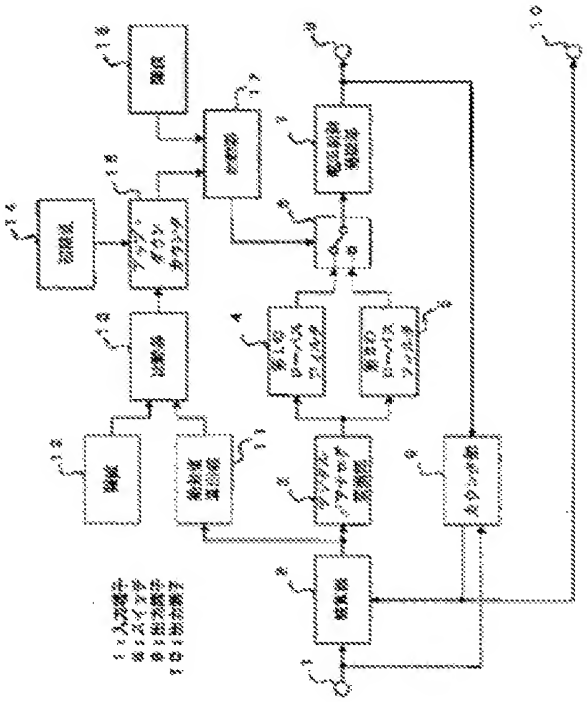
5J106

5K047
F-term (reference)

5J106 AA04 BB02 BB04 CC01 CC26 CC38 CC41 CC52 DD09 DD19 DD36 DD44 EE10 FF02 GG07 HH10 JJ09 KK05 KK25 LL07

5K047 AA06 CC08 GG09 GG45 MM33 MM35 MM46 MM50 MM58 MM63

Abstract:
PROBLEM TO BE SOLVED: To obtain a phase locked loop capable of suppressing phase jitter and preventing the clock signal from being suddenly changed even when a clock signal causing the phase jitter is given to a decoder, thereby conducting stable decoding.SOLUTION: The phase locked loop that applies synchronization processing to a clock signal used by a decoder on the basis of a phase of the clock signal used by the decoder with a phase of reference time information included in an input signal, is provided with discrimination means 11-17 that discriminate whether or not the input signal is a signal causing phase jitter to the clock signal and with revision means 4-8 that revise response sensitivity of the synchronization processing on the basis of the result of discrimination by the discrimination means.



JPO Machine translation abstract:

(57) **Abstract**

SUBJECT Even when the signal which produces phase fluctuation (jitter) is inputted into the clock used by a decoder, fluctuation of a phase can be controlled, the abrupt change of a clock signal can be prevented, and the phase synchronization circuit which can perform stable decode operation is obtained.

Means for Solution In a phase synchronization circuit which performs synchronous processing of said clock signal based on a difference value of a phase of a clock signal used by the decoder side, and a phase of base period information included in an input signal, Said input signal is provided with the judging means 11-17 which judge whether it is a signal which makes a phase of said clock signal produce fluctuation, and the alteration means 4-6 which change response sensitivity of synchronous processing based on a decided result of said judging means.

Claim(s)

Claim 1A phase synchronization circuit which performs synchronous processing of said clock signal based on a difference value of a phase of a clock signal used by the decoder side characterized by comprising the following, and a phase of base period information included in an input signal.
A judging means which judges whether said input signal is a signal which makes a phase of said clock signal produce fluctuation.
An alteration means which changes response sensitivity of synchronous processing based on a decided result of said judging means.

Claim 2 The phase synchronization circuit according to claim 1 when said alteration means is **said input signal** a signal which makes a phase of said clock signal produce fluctuation, wherein it makes response sensitivity of synchronous processing lower than a specified value.

Claim 3 When a period when said judging means becomes larger than a threshold value with an absolute value of said difference value continues more than a prescribed period, Or the phase synchronization circuit according to claim 1 judging with said input signal being a signal which makes a phase of said clock signal produce fluctuation when probability which becomes larger than a threshold value with said absolute value becomes beyond a specified value.

Claim 4 The phase synchronization circuit comprising according to claim 1:
An absolute value calculation part in which said judging means computes an absolute value of said difference value.
An updown counter which carries out down counting of the computed difference absolute value as compared with the 1st threshold value in being larger than the 1st threshold value, and being small, a rise count and.
Counted value of said updown counter is judged as said input signal being a signal which makes a phase of said clock signal produce fluctuation as compared with the 2nd threshold value, when larger than the 2nd threshold value, A comparator judged as said input signal not being a signal which makes a phase of said clock signal produce fluctuation when small.

Claim 5 The phase synchronization circuit comprising according to claim 1:
An absolute value calculation part in which said judging means computes an absolute value of said difference value.
Smooth sections which predetermined-number-collection-********** a computed difference absolute value.
A control signal generating section which judges a grade from which said input signal makes a phase of said clock signal produce fluctuation according to size of an output of said smooth sections, and generates a control signal according to a decided result.

Claim 6 Said judging means considers data showing effective and invalidity of an input signal as an input, The phase synchronization circuit according to claim 1 judging with said input signal being a signal which makes a phase of said clock signal produce fluctuation when a period when invalid data is inputted continues more than a prescribed period, or when

probability that invalid data will be inputted becomes beyond a specified value.
Claim 7 The phase synchronization circuit comprising according to claim 1:
An updown counter which carries out down counting in being small, a rise count and whenever said judging means asks for a period which invalid data inputs by considering data showing effective and invalidity of an input signal as an input, and invalid data inputs a period for which it asked, in being larger than the 1st threshold value as compared with the 1st threshold value. Counted value of said updown counter is judged as said input signal being a signal which makes a phase of said clock signal produce fluctuation as compared with the 2nd threshold value, when larger than the 2nd threshold value, A comparator judged as said input signal not being a signal which makes a phase of said clock signal produce fluctuation when small.

Claim 8 Smooth sections which predetermined-number-collection-********** a period which said judging means considers data showing effective and invalidity of an input signal as an input, and invalid data inputs, The phase synchronization circuit according to claim 1 where said input signal is characterized by having a control signal generating section which judges a grade which makes a phase of said clock signal produce fluctuation, and outputs a control signal according to a decided result according to size of an output of said smooth sections.
Claim 9 The phase synchronization circuit according to claim 1 making a change of response sensitivity in said alteration means by change of a pass band of a low pass filter used for synchronous processing.
Claim 10 The phase synchronization circuit according to claim 1 making a change of response sensitivity in said alteration means by change of a multiplication coefficient of a coefficient unit used for synchronous processing.
Claim 11 Smooth sections which predetermined-number-collection-********** a period which considers data showing effective and invalidity of an input signal as an input, and when invalid data inputs it, The phase synchronization circuit according to claim 1 provided with the amount calculation part of time gaps which computes the amount of time gaps of said clock signal based on an output of said smooth sections, and a compensation means which said clock signal amends based on the computed amount of time gaps.

Detailed Description of the Invention
0001
Field of the Invention The digital broadcasting for which this invention uses a broadcasting satellite and a terrestrial wave, the cable TV using a cable. (It is hereafter described as CATV) It is related with the phase synchronization circuit used for the MPEG decoder etc. which restore to the program stream or transport stream compressed by the MPEG standard used with broadcast or DVD.
0002
Description of the Prior Art Drawing 10 is a block diagram of the digital satellite broadcasting receiver which uses the conventional MPEG decoder currently generally used. The input terminal into which 101 inputs an input signal in a figure, the tuner module into which 102 inputs the input signal from the input terminal 1, The descrambler to which 103 considers the output from the tuner module 102 as an input, The MPEG demultiplexer to which 104 considers the output from the descrambler 103 as an input, The MPEG video decoder to which 105 considers the output from the MPEG demultiplexer 104 as an input, The MPEG audio decoders to which 106 considers the output from the MPEG demultiplexer 104 as an input, The NTSC encoder with which 107 considers the output from MPEG video decoder 105 as an input, The output terminal in which 108 outputs an NTSC signal, the D/A converter to which 109 considers the output from MPEG audio decoders as an input, the output terminal in which 110 outputs an analog voice signal, and 111 are CPUs for control.
0003 Explanation of signal processing in a receiver will input first the satellite wave which received with the satellite dish for passing tuner module 102 from the input terminal 101. The tuner module 102 performs decoding of the change of receiving transponders, a recovery, and an error correction, etc., and extracts the MPEG transport stream which the individual data row (stream) multiplexed. It is inputted into the descrambler 103, code release is carried out, and this transport stream (it is hereafter described as TS) is transmitted to the MPEG demultiplexer 104. Program specification information based on a televiewer's channel selection operation in the MPEG demultiplexer 104 (below Program Specific Information:.) PSI -- describing -- it receives, required picture image data and voice data are extracted from TS, and it sends out to MPEG video decoder 105 and MPEG audio decoders 106. MPEG video decoder 105 cancels compression of picture image data, changes it into an NTSC signal with NTSC encoder 107, and outputs an NTSC signal to a television set from the output terminal 108. MPEG audio decoders 106 cancel compression of voice data, change it into an analog voice signal by D/A converter 109, and are outputted to a television set from the output terminal 110. CPU111 for control controls processing of these series.
0004 Also in CATV, the digital signal received via the cable is carried out in the same processing as the above, and is outputted to a television set. Thus, the MPEG demultiplexer 104 has a function which decomposes TS of MPEG contained in the satellite wave which received into picture image data, audio information, and other control data. It also has the function which regenerates the clock signal used with the MPEG demultiplexer 104, MPEG video decoder 105, MPEG audio decoders 106, and NTSC encoder 107 by one side.
0005 The MPEG encoder (coding equipment) which codes and compresses picture image data and voice data by the broadcasting organization side with regeneration of this clock signal, It is time management, i.e., the processing which takes a synchronization, common between the MPEG decoders (decoding device) which cancel compression of picture image data or voice data by the televiewer side. Next, regeneration of a clock signal is explained.
0006 Drawing 11 is a block diagram showing the composition of the phase synchronization circuit used for regeneration of a clock signal. The input terminal into which a TS signal inputs 1 in a figure, the program time reference value included in the TS signal which inputted 2 from the input terminal 1 (below ProgramClock Reference:.) The value of the synchronized signal which is outputted from the counter section 9 mentioned later from describing it as PCR and which serves as a time standard in an MPEG decoder (below System Time Clock:.) STC -- describing -- the subtraction part (phase-comparison part) to subtract and 3 change into an analog signal the digital signal which the subtraction part 2 outputs -- a digital/analog conversion part. (It is hereafter described as a D/A conversion part), the 1st low pass filter to which 4 considers the output of the D/A conversion part 3 as an input. (It is hereafter described as the 1st LPF), the voltage control oscillation part (below Voltage Control Oscillator: describes it as VCO) to which 7 considers the output of 1st LPF4 as an input, the output terminal in which 8 outputs a clock to a latter-part circuit. 9 is a counter section which counts the clock which VCO7 outputs.
0007PCR which was extracted and was separated from TS is used for regeneration of the clock signal in a phase synchronization circuit. In the MPEG decoder containing the video decoder 105 and the audio decoder 106, this PCR is the

information for setting it as a 27-MHz clock frequency, and amending in the case of the value which meant the value of STC by the MPEG encoder side by the side of a broadcast contractor, i.e., MPEG 2.
It is contained by a length of 42 bits in the specific stream.
If regeneration of the clock signal CLK is explained, the value of PCR first extracted from the specific stream will be written in the counter section 9 as it is (setting up), and STC and PCR which are outputted from the counter section 9 will be initialized as a synchronous state (the same value). The counter 9 makes an initial value written-in PCR, and counts and counts up the receive clock outputted from VCO7. An input of following PCR will perform subtraction treatment with STC from the counter section 9 when PCR is received in the subtraction part 2. When the phase of the clock signal of PCR and STC both is thoroughly in agreement, the output of a subtraction part is set to 0. On the other hand, when both phase is different, the difference is changed into a voltage signal via the D/A conversion part 3 and the 1st LPF4, and it is impressed by VCO7. Phase correction of the CLK is carried out by amending the frequency of the clock signal CLK outputted from VCO7 by this voltage signal. Since the counter section 9 is constituted so that it may count up with the clock signal CLK outputted from VCO7, counted value, i.e., the phase of STC, is controlled according to the output change of VCO7.
0008 Thus, the phase of the clock signal CLK by the side of an MPEG decoder can be correctly coincided the MPEG encoder side by regenerating a clock signal based on PCR. Therefore, the data volume of the buffer memory provided in the video decoder 105 and the audio decoder 106 by being attached overflows, It can prevent that it will be in an underflow state, and the synchronization of the picture image data and voice data using the time-of-day-control information on a reproducing output (below Presentation Time Stamp: describes it as PTS) can be taken. Regeneration of the clock signal by such a phase synchronization circuit is premised on PCR in a stream being generated correctly.
0009
Problem to be solved by the invention By the way, the structure of the packet (transport stream packet: it is hereafter described as a TS packet) which carried out time multiplexing of many individual streams, A video elementary stream, the packet elementary stream having contained the audio elementary stream (below Packetized Elementary Stream:.) It has a multiplex layered structure included from PSI, PCR, etc. on the packet described as PES, and a different class from a PES packet.
0010 Therefore, when generating a TS packet directly from data inputted into the MPEG encoder side, can perform creating and inserting PCR easily, but. If only data of an elementary stream or a PES packet tends to be compounded and it is going to generate a TS packet, Since PCR is contained on a level of a TS packet, a phase of a clock when elementalist ream is created is not reflected, and it cannot be inserted **can create exact PCR and** .
0011 In order to carry out multiplex and to transmit by other information and time sharing from a relation of a communications network, when a communications network which gathers and transmits access speed is passed, in the transmitting side. Time is read from a counter clocked based on a clock of reference frequency from a source of a transmitting reference clock at a random interval, and it is transmitted to a communications network as time information PCR.
0012 This time information PCR is read from a counter at intervals of **random** less than 100 ms of predetermined intervals, and that value shows the time T from the last read-out. In a receiver, time information is received as receiving time information via the above-mentioned communications network, and a receive clock is reproduced by phase synchronization circuit. When a transmission signal gathered and transmits access speed at this time, time compression of the TS data will be carried out to a period shown by the above-mentioned valid data period signal with a valid data period signal, they will be transmitted burstily, a time lag produces them in time information, and the arrival time of receiving time information is changed. Although the above explained TS, The same may be said of a case of a program stream, and it is a system time standard reference value in the case of the above-mentioned program stream (below System Clock Reference:.). SCR -- describing -- it is similarly read from a counter at intervals of **random** less than 700 ms of predetermined intervals, and the value shows the time T from the last read-out. In a receiver, time information is received as receiving time information via the above-mentioned communications network, and a receive clock is reproduced by phase synchronization circuit.
0013 Change of the above arrival time of time information appeared as fluctuation of the phase of STC (jitter), and since fluctuation of this kind of phase could not be controlled, the transmission signal in the above communications networks had the problem that stable receiving operation could not be performed in the conventional phase synchronization circuit.
0014 Although the buffer of the received data is carried out to dissolution of the above problems and the method of transmitting at a fixed rate approximately from a buffer using the transmission rate shown in the syntax of received data is indicated in ITUT-T advice H.220.0, Since the above-mentioned transmission rate did not necessarily show the exact rate, it had the problem that the sufficiency degree of the data in a buffer had to be supervised and controlled in addition to adding a buffer.
0015 By reproducing a clock with accuracy sufficient even when it was made in order that this invention might cancel above SUBJECT, and fluctuation of a phase occurs near the sampling frequency, While being able to prevent the data volume of the buffer memory provided in the video decoder 105 and the audio decoder 106 by being attached from being in overflow and an underflow state, It aims at providing the phase synchronization circuit which can take the synchronization of the picture image data and voice data using PTS of the reproducing output.
0016
Means for solving problem The phase synchronization circuit which this invention requires for this invention is characterized by that the phase synchronization circuit which performs synchronous processing of said clock signal based on the difference value of the phase of the clock signal used by the decoder side and the phase of the base period information included in an input signal comprises:
The judging means which judges whether said input signal is a signal which makes the phase of said clock signal produce fluctuation.
The alteration means which changes the response sensitivity of synchronous processing based on the decided result of said judging means.

0017 The phase synchronization circuit concerning this invention was constituted so that it might make response sensitivity of synchronous processing lower than a specified value, in being a signal with which said input signal makes the phase of said clock signal produce fluctuation for said alteration means.
0018 When the period when the phase synchronization circuit concerning this invention becomes larger than a threshold value with the absolute value of said difference value about said judging means continues more than a prescribed period, Or when the probability which becomes larger than a threshold value with said absolute value became beyond a specified value,

it constituted so that it might judge with said input signal being a signal which makes the phase of said clock signal produce fluctuation.

0019 The absolute value calculation part in which the phase synchronization circuit concerning this invention computes the absolute value of said difference value for said judging means, The updown counter which carries out down counting of the computed difference absolute value as compared with the 1st threshold value in being larger than the 1st threshold value, and being small, a rise count and, The counted value of said updown counter is judged as said input signal being a signal which makes the phase of said clock signal produce fluctuation as compared with the 2nd threshold value, when larger than the 2nd threshold value, When small, said input signal consisted of comparators judge that are not the signals which make the phase of said clock signal produce fluctuation.

0020 An absolute value calculation part in which a phase synchronization circuit concerning this invention computes an absolute value of said difference value for said judging means, According to size of an output of smooth sections which predetermined-number-collection-********** a computed difference absolute value, and said smooth sections, said input signal judged a grade which makes a phase of said clock signal produce fluctuation, and consisted of control signal generating sections which generate a control signal according to a decided result.

0021A phase synchronization circuit concerning this invention considers as an input data which expresses effective and invalidity of an input signal for said judging means, When a period when invalid data is inputted continued more than a prescribed period, or when probability that invalid data will be inputted became beyond a specified value, it constituted so that it might judge with said input signal being a signal which makes a phase of said clock signal produce fluctuation.

0022A phase synchronization circuit concerning this invention considers as an input data which expresses effective and invalidity of an input signal for said judging means, An updown counter which carries out down counting in being small, a rise count and whenever it asks for a period which invalid data inputs, and invalid data inputs a period for which it asked, in being larger than the 1st threshold value as compared with the 1st threshold value, Counted value of said updown counter is judged as said input signal being a signal which makes a phase of said clock signal produce fluctuation as compared with the 2nd threshold value, when larger than the 2nd threshold value, When small, said input signal consisted of comparators judge that are not the signals which make a phase of said clock signal produce fluctuation.

0023 The smooth sections which predetermined-number-collection-********** the period which the phase synchronization circuit concerning this invention considers as an input the data which expresses effective and the invalidity of an input signal for said judging means, and invalid data inputs, According to the size of the output of said smooth sections, said input signal judged the grade which makes the phase of said clock signal produce fluctuation, and consisted of control signal generating sections which output the control signal according to a decided result.

0024 The phase synchronization circuit concerning this invention was constituted so that a change of the response sensitivity in said alteration means might be made by change of the pass band of the low pass filter used for synchronous processing.

0025 The phase synchronization circuit concerning this invention was constituted so that a change of the response sensitivity in said alteration means might be made by change of the multiplication coefficient of the coefficient unit used for synchronous processing.

0026 The smooth sections which predetermined-number-collection-********** the period which the phase synchronization circuit concerning this invention considers the data showing effective and the invalidity of an input signal as an input, and invalid data inputs, It constituted so that it might have further the amount calculation part of time gaps which computes the amount of time gaps of said clock signal based on the output of said smooth sections, and a compensation means which said clock signal amends based on the computed amount of time gaps.

0027

Mode for carrying out the invention Hereafter, this invention is concretely explained based on the Drawings in which that embodiment is shown.

Embodiment 1. drawing 1 shows the phase synchronization circuit of the MPEG data receiver which is this embodiment of the invention 1. The input terminal into which PCR contained in a TS signal inputs 1 in the figure, The subtraction part which subtracts STC outputted from the counter section 9 mentioned later from PCR which 2 inputted, The D/A conversion part which changes into an analog signal the digital signal value to which the subtraction part 2 outputs 3, The 1st LPF to which 4 considers the output of the D/A conversion part 3 as an input, the 2nd LPF to which five consider the output of the D/A conversion part 3 as an input, 6 is a switch part which changes and outputs the output of 1st LPF4, and the output of 2nd LPF5 based on the output of the comparator 17 mentioned later, and the response sensitivity of a phase synchronization circuit is changed by this switch part. VCO to which 7 considers the output of the switch part 6 as an input, the output terminal which outputs the receive clock which outputs eight from VCO, The counter section which counts the receive clock which outputs 9 from VCO, the output terminal which outputs STC which outputs 10 from the counter section 9 to the latter part, The absolute value calculation part which considers the digital signal value which outputs 11 from the subtractor 2 as an input, The threshold value 12 indicates any value to be, the comparator to which 13 considers the output and the threshold value 12 of the absolute value calculation part 11 as an input, The initial value of the updown counter 15 which 14 mentions later, the updown counter to which 15 considers the output and the initial value 14 of the comparator 13 as an input, the threshold value 16 indicates any value to be, and 17 are comparators which consider the output and the threshold value 16 of the updown counter 15 as an input. The absolute value calculation part 11 thru/or the comparator 17 constitute a judging means.

0028 The subtraction part 2 performs subtraction treatment of PCR inputted from the input terminal 1, and STC outputted from the counter section 9. When the phase of the clock signal of PCR and STC both is thoroughly in agreement, the output of the subtraction part 2 is set to 0. On the other hand, when both phase is different, the difference value outputs to the D/A conversion part 3 and the absolute value calculation part 11. The 1st LPF4 that differed in the characteristic changed by the switch part 6 by the decision signal from a judging means, and the 2nd LPF5 are in the output of the D/A conversion part 3, it is worn, is changed into a voltage signal via ** one side, and is impressed to VCO7. By amending the frequency of a receive clock with said voltage signal, VCO7 amends a phase and it outputs it to the output terminal 8. Since the counter section 9 is constituted so that the receive clock outputted from VCO7 may be counted up, counted value, i.e., the phase of STC, is controlled according to the output change of VCO7.

0029 The absolute value calculation part 11 computes the absolute value of the difference value outputted from the subtraction part 2, when the absolute value of this difference value is larger than the arbitrary threshold values 12 with the comparator 13, whenever PCR comes, it makes the updown counter 15 count up, and when small, it is made to count down. The comparator 17 changes the switch part 6 so that a voltage signal may pass the 1st LPF4 **same** as a conventional example, when the counted value of the updown counter 15 is smaller than the arbitrary threshold values 16, The switch part

6 is changed so that a voltage signal may pass the 2nd LPF5 that passes only a lower zone compared with the 1st LPF4, in being large. The updown counter 15 shall initialize an initial value, whenever new TS is inputted and a phase synchronization circuit starts synchronous processing.

0030A time lag arises at the arrival time of PCR by time compression of the TS data being carried out by transmission signal processing etc., and transmitting them burstily by the above operation, If the value of the counter 15 of an updown counter will become large if the probability that the absolute value of the difference value of above-mentioned PCR and STC of an MPEG decoder will be computed more greatly than the arbitrary threshold values 12 increases, and this value becomes larger than the arbitrary threshold values 16, A judging means judges with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, and changes LPF which is a loop filter of a phase synchronization circuit to the 2nd LPF5 that is low sensitivity. Thereby, a phase synchronization circuit performs synchronous processing which carries out a low sensitivity response, and can control fluctuation of a phase.

0031 Embodiment 2. drawing 2 shows the phase synchronization circuit of the MPEG data receiver which is this embodiment of the invention 2. The input terminal which inputs the valid data period signal which shows the period when valid data is inputted in the figure among the TS signals which 18 inputs, The counter section which considers as an input the valid data period signal which inputs 19 from the input terminal 18, The threshold value 20 indicates any value to be, the comparator to which 21 considers the output and the threshold value 20 of the counter section 19 as an input, The threshold value 22 indicates any value to be, the initial value of the updown counter 23 which 22 mentions later, the updown counter to which 23 considers the output and the initial value 22 of the comparator 21 as an input, the threshold value 24 indicates arbitration to be, and 25 are comparators which consider the output and the threshold value 24 of the updown counter 23 as an input. A judging means is constituted by the counter section 19 thru/or the comparator 25.

0032 The counter section 19 counts with a receive clock with the time as the starting point of the input start of the invalid data being carried out using the valid data period signal which shows the period when valid data is inputted among the TS signals inputted from the input terminal 18, and evaluates invalid period width as counted value of a receive clock. When the evaluated invalid period width has the large invalid period width which was compared with the threshold values 20 with an arbitrary twist, and was evaluated by the comparator 21, whenever invalid data is inputted, the updown counter 23 is made to count up, and it is made to count down when small. The comparator 25 changes the switch part 6 so that a voltage signal may pass the 1st LPF4 **same** as a conventional example, when the counted value of the updown counter 23 is smaller than the arbitrary threshold values 24, The switch part 6 is changed so that a voltage signal may pass the 2nd LPF5 that passes only a lower zone compared with the 1st LPF4, in being large. The updown counter 23 shall initialize an initial value, whenever TS is inputted and a phase synchronization circuit starts synchronous processing.

0033 When a signal which a time lag produces at the arrival time of PCR by time compression of the TS data being carried out by the above operation, and transmitting them burstily by it is inputted, If the frequency which comes using the valid data period signal which shows the period when valid data is inputted among TS signals by width with larger invalid period width than the arbitrary threshold values 20 becomes high, counter 23 value of an updown counter will become large, If this value becomes larger than the arbitrary threshold values 24, a judging means will judge with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, and will change LPF which is a loop filter of a phase synchronization circuit to the 2nd LPF5 that is low sensitivity. Thereby, a phase synchronization circuit performs synchronous processing which carries out a low sensitivity response, and can control fluctuation of a phase.

0034 Embodiment 3. drawing 3 shows the phase synchronization circuit of the MPEG data receiver which is this embodiment of the invention 3. The 1st coefficient unit with which 26 considers the output of the subtractor 2 as an input in the figure, the 2nd coefficient unit with which 27 considers the output of the subtractor 2 as an input, 28 is a selector which changes the output of the 1st coefficient unit 26, and the output of the 2nd coefficient unit 27 based on the output of the comparator 17, and the response sensitivity of a phase synchronization circuit is changed by this selector. The adding machine with which 29 considers the output of the selector 28 and the output of a D flip-flop mentioned later as an input, and 30 are D flip-flops which consider the output of the adding machine 29 as an input. About a judging means, it is the same as that of what was explained by Embodiment 1.

0035 The 1st coefficient unit 26 carries out the multiplication of the coefficient A of $0< A<1$ to the difference value of the subtractor 2, and the 2nd coefficient unit 27 carries out the multiplication of the coefficient B of $0<B<A<1$. The selector 28 chooses the difference value by which multiplication was carried out with the 1st coefficient unit, when the counted value of the updown counter 15 is smaller than the arbitrary threshold values 16, and when large, it chooses the difference value by which multiplication was carried out with the 2nd coefficient unit. The adding machine 29 adds the difference value by which multiplication was carried out by one of coefficients, and the digital value of the control voltage outputted from D flip-flop 30 mentioned later. D flip-flop 30 is memorized to timing each time the digital value of the control voltage outputted from the adding machine 29 is inputted into PCR. The D/A conversion part 3 changes into a voltage signal the value memorized by the D flip-flop, and impresses it to VCO7.

0036A time lag arises at the arrival time of PCR by time compression of the TS data being carried out by the above operation, and transmitting them burstily by it, If the probability that the absolute value of a difference value with STC which is a value of the synchronized signal used as above-mentioned PCR and the time standard of an MPEG decoder will be computed more greatly than the arbitrary threshold values 12 increases, the value of the counter 15 of an updown counter will become large, When this value becomes larger than the arbitrary threshold values 16, a judging means, It judges with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, and the 1st coefficient unit 26 of a phase synchronization circuit, the adding machine 29, and the coefficient unit of the digital gone type loop filter constituted from D flip-flop 30 are changed to the 2nd coefficient unit that carries out multiplication by a smaller coefficient. Thereby, a phase synchronization circuit performs synchronous processing which carries out a low sensitivity response, and can control fluctuation of a phase.

0037 Embodiment 4. drawing 4 shows the phase synchronization circuit of the MPEG data receiver which is this embodiment of the invention 4. In the figure, 28 is a selector which changes the output of the 1st coefficient unit 26, and the output of the 2nd coefficient unit 27 based on the output of the comparator 25, and the response sensitivity of a phase synchronization circuit is changed by this selector. The judging means is the same as that of Embodiment 2.

0038 The selector 28 chooses the difference value by which multiplication was carried out with the 1st coefficient unit, when the counted value of the updown counter 23 is smaller than the arbitrary threshold values 24, and when large, it chooses the difference value by which multiplication was carried out with the 2nd coefficient unit.

0039 When a signal which a time lag produces at the arrival time of PCR by time compression of the TS data being carried out by the above operation, and transmitting them burstily by it is inputted, If the frequency which comes using the valid

data period signal which shows the period when valid data is inputted among TS signals by width with larger invalid period width than the arbitrary threshold values 20 becomes high, counter 23 value of an updown counter will become large, If this value becomes larger than the arbitrary threshold values 24, a judging means will judge with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, The 1st coefficient unit 26 of a phase synchronization circuit, the adding machine 29, and the coefficient unit of the digital gone type loop filter constituted from D flip-flop 30 are changed to the 2nd coefficient unit that carries out multiplication by a smaller coefficient. Thereby, a phase synchronization circuit performs synchronous processing which carries out a low sensitivity response, and can control fluctuation of a phase.

0040 Embodiment 5. drawing 5 shows the phase synchronization circuit of the MPEG data receiver which is this embodiment of the invention 5. The smooth sections to which 31 considers the output of the absolute value calculation part 11 as an input in the figure, The control signal generating section to which 32 considers the output of the smooth sections 31 as an input, and 33 are coefficient-of-variable-capacitance machines which change the coefficient which carries out multiplication to the output of the subtractor 2 based on the output of the control signal generating section 32, and the response sensitivity of a phase synchronization circuit is changed with this coefficient-of-variable-capacitance machine. 29 is an adding machine adding the output and D flip-flop 30 of the coefficient-of-variable-capacitance machine 33. The absolute value calculation part 11, the smooth sections 31, and the control signal generating section 32 constitute a judging means.

0041 The coefficient-of-variable-capacitance machine 33 carries out the multiplication of the coefficient X of 0< X<1 to the difference value of the subtractor 2. The coefficient X is gradually changed by the control signal outputted from the control signal generating section 32 mentioned later. The adding machine 29 adds the difference value by which multiplication was carried out with the coefficient-of-variable-capacitance machine, and the digital value of the control voltage outputted from D flip-flop 30 mentioned later. D flip-flop 30 is memorized to timing each time the digital value of the control voltage outputted from the adding machine 29 is inputted into PCR. The D/A conversion part 3 changes into a voltage signal the value memorized by D flip-flop 30, and impresses it to VCO7.

0042 The absolute value calculation part 11 computes the absolute value of the difference value outputted from said subtraction part 2, and carries out smoothness of the absolute value of the difference value in which number-of-times calculation of arbitrary was carried out by the smooth sections 31. The control signal generating section 32 generates the control signal according to the value outputted from the smooth sections 31. The coefficient-of-variable-capacitance machine 33 changes a coefficient gradually so that the value outputted from the smooth sections 31 is large, and the coefficient X may become small.

0043A time lag arises at the arrival time of PCR by time compression of the TS data being carried out by the above operation, and transmitting them burstily by it, A difference value with STC which is a value of the synchronized signal used as above-mentioned PCR and the time standard of an MPEG decoder is computed, If smoothness of the absolute value of the difference value is carried out by a part for the number of times of arbitrary and the value becomes large, a judging means will judge with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, It is made to carry out the multiplication of the coefficient which changed gradually the coefficient of the digital gone type loop filter constituted from the multistage coefficient unit 33, the adding machine 29, and D flip-flop 30 of a phase synchronization circuit, and changed it according to the value. Thereby, warm synchronous processing can be performed and fluctuation of a phase is controlled rather than a phase synchronization circuit carries out the low sensitivity response according to the state of the TS data inputted. A phase synchronization circuit may be constituted like Embodiment 1, and although the case where the multiplication coefficient of the coefficient-of-variable-capacitance machine 33 was changed based on the output of the control signal generating section 32 was explained, it may constitute from this embodiment so that switching control of the pass band of LPF may be carried out.

0044 Embodiment 6. drawing 6 shows the phase synchronization circuit of the MPEG data receiver which is this embodiment of the invention 6. The smooth sections to which 34 considers the output of the counter section 19 as an input in the figure, the control signal generating section to which 35 considers the output of the smooth sections 34 as an input, 33 is a coefficient-of-variable-capacitance machine which changes the coefficient which carries out multiplication to the output of the subtractor 2 based on the output of the control signal generating section 35, and the response sensitivity of a phase synchronization circuit is changed with this coefficient-of-variable-capacitance machine. The counter section 19, the smooth sections 34, and the control signal generating section 35 constitute a judging means.

0045 The smooth sections 34, Smoothness of the invalid period width counted and evaluated with the receive clock with the time as the starting point of the input start of the invalid data being carried out using the valid data period signal which shows the period when valid data is inputted among the TS signals counted by the counter section 19 is carried out by a part for the number of times of arbitrary at which invalid data arrived. The control signal generating section 35 generates a control signal according to the value outputted from the smooth sections 34. The coefficient-of-variable-capacitance machine 33 changes a coefficient gradually so that the value outputted from the smooth sections 35 is large, and the coefficient X may become small.

0046 When a signal which a time lag produces at the arrival time of PCR by time compression of the TS data being carried out by the above operation, and transmitting them burstily by it is inputted, Invalid period width is predetermined-number-collection-********(ed) using the valid data period signal which shows the period when valid data is inputted among TS signals. And if the value becomes large, a judging means will judge with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, The multiplication of the coefficient which changed gradually the coefficient of the digital gone type loop filter constituted from the coefficient-of-variable-capacitance machine 33, the adding machine 29, and D flip-flop 30 of a phase synchronization circuit, and changed it according to the value is carried out. rather than a phase synchronization circuit carries out the low sensitivity response according to the state of the TS data inputted by this -- texture -- warm synchronous processing can be performed and fluctuation of a phase can be controlled. A phase synchronization circuit may be constituted like Embodiment 2, and although the case where the multiplication coefficient of the coefficient-of-variable-capacitance machine 33 was changed based on the output of the control signal generating section 35 was explained, it may constitute from this embodiment so that switching control of the pass band of LPF may be carried out.

0047 Embodiment 7. drawing 7 shows the phase synchronization circuit of the MPEG data receiver which is this embodiment of the invention 7. The smooth sections to which 34 considers the output of the counter section 19 as an input in the figure, the amount calculation part of time gaps to which 36 considers the output of the smooth sections 34 as an input, The adding machine with which 37 considers the output of STC which is an output from the counter section 9, and the amount calculation part 36 of time gaps as an input, and 10 are output terminals which output amended STC which is outputted from the adding machine 37 to the latter part. Since the composition of those other than smooth-sections 34, amount calculation part 36 of time gaps, and adding machine 37 is the same as that of Embodiment 2, detailed explanation is omitted.

0048 The smooth sections 34, Smoothness of the invalid period width counted and evaluated with the receive clock with the time as the starting point of the input start of the invalid data being carried out using the valid data period signal which shows the period when valid data is inputted among the TS signals counted by the counter section 19 is carried out by a part for the number of times of arbitrary at which invalid data arrived. The amount calculation part 36 of time gaps computes the time lag of the arrival time of PCR produced by time compression of the TS data being carried out, and being burstily transmitted from the evaluated invalid period width which is outputted from the smooth sections 34, converts this time lag into the counted value of a receive clock, and outputs it. The adding machine 37 functions as a compensation means which adds STC outputted from the counter 9, and the time lag converted into the counted value of the receive clock outputted from the amount calculation part 36 of time gaps, and outputs it to the latter part as an amended STC.
0049 When a signal which a time lag produces at the arrival time of PCR by time compression of the TS data being carried out by the above operation, and transmitting them burstily by it is inputted, If the frequency which comes using the valid data period signal which shows the period when valid data is inputted among TS signals by width with larger invalid period width than the fixed threshold value 20 becomes high, counter 23 value of an updown counter will become large, If this value becomes larger than the arbitrary threshold values 24, a judging means will judge with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, and will change LPF which is a loop filter of a phase synchronization circuit to the 2nd LPF5 that is low sensitivity. Smoothness of the invalid period width is carried out by a part for the number of times of arbitrary at which invalid data arrived (smooth sections 34), the amount of time gaps of STC which made it generate by a phase synchronization circuit based on this value is computed (the amount calculation part 36 of time gaps), and correction value is added in the adding machine 37. A time gap of STC which performed synchronous processing which carries out a response **low sensitivity phase synchronization circuit** by these operations, and could control fluctuation of a phase, and was generated in the phase synchronization circuit can be amended and MPEG-decoded.
0050 Embodiment 8. drawing 8 shows the phase synchronization circuit of the MPEG data receiver which is this embodiment of the invention 8. The composition except the smooth sections 34, the amount calculation part 36 of time gaps, and the adding machine 37 is the same as that of drawing 4 explained in Embodiment 4 so that clearly from a figure.
0051 It is the same and operation is explained briefly hereafter as Embodiments 4 and 7 mentioned above explained. When a signal which a time lag produces by carrying out time compression of the TS data, and transmitting them burstily at the arrival time of PCR is inputted, If the frequency which comes using the valid data period signal which shows the period when valid data is inputted among TS signals by width with larger invalid period width than the arbitrary threshold values 20 becomes high, counter 23 value of an updown counter will become large, If this value becomes larger than the arbitrary threshold values 24, a judging means will judge with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, The 1st coefficient unit 26 of a phase synchronization circuit, the adding machine 29, and the coefficient unit of the digital gone type loop filter constituted from D flip-flop 30 are changed to the 2nd coefficient unit that carries out multiplication by a smaller coefficient. Smoothness of the invalid period width is carried out by a part for the number of times of arbitrary at which invalid data arrived, the amount of time gaps of STC which made it generate by a phase synchronization circuit based on this value is computed, and this correction value is added in the adding machine 37. While performing synchronous processing which carries out a response **low sensitivity phase synchronization circuit** by these operations and being able to control fluctuation of a phase, a time gap of STC generated in the phase synchronization circuit can be amended and MPEG-decoded.
0052 Embodiment 9. drawing 9 shows a phase synchronization circuit of an MPEG data receiver which is this embodiment of the invention 9. Composition except the amount calculation part 36 of time gaps and the adding machine 37 is the same as that of drawing 6 explained in Embodiment 6 so that clearly from a figure.
0053 It is the same and operation is explained briefly hereafter as Embodiments 6 and 7 mentioned above explained. When a signal which a time lag produces by carrying out time compression of the TS data, and transmitting them burstily at the arrival time of PCR is inputted, invalid period width is predetermined-number-collection-********(ed) using a valid data period signal which shows a period when valid data is inputted among TS data. And if the value becomes large, a judging means will judge with TS data which produce fluctuation of a phase of STC (jitter) being inputted, Multiplication is carried out by calculation which changed gradually a coefficient of a digital gone type loop filter constituted from the multistage coefficient unit 33, the adding machine 29, and D flip-flop 30 of a phase synchronization circuit, and changed it according to the value. Smoothness of the invalid period width is carried out by a part for the number of times of arbitrary at which invalid data arrived, the amount of time gaps of STC generated by a phase synchronization circuit based on this value is computed, and that correction value is added in the adding machine 37. A time gap of STC which performed synchronous processing which carries out a low sensitivity response according to a state of TS data where a phase synchronization circuit is inputted by these operations, and could control fluctuation of a phase, and was generated in a phase synchronization circuit can be amended and MPEG-decoded.
0054 Although Embodiments 1-9 explain by extracting and processing PCR contained in the TS signal by setting an input signal to TS, an effect also with same also extracting and processing SCR contained in a program stream by making an input signal into a program stream is acquired. Although the above-mentioned Embodiments 7-9 explained what provided the circuit for STC amendment (the smooth sections 34, the amount calculation part of time gaps, the adding machine 37) to the phase synchronization circuit of Embodiments 2, 4, and 6, naturally it may be made to provide to the phase synchronization circuit of Embodiments 1, 3, and 5. For example in the phase synchronization circuit of drawing 1, drawing 3, and drawing 5, namely, the valid data period signal input terminal 18, the counter section 19, the smooth sections 34, the amount calculation part of time gaps, It connects so that the adding machine 37 may be added, the output of VCO7 may be made to input also into the counter 19 and the adding machine 37 may be made to be placed between from the subtractor 2 before the output terminal 10.
0055
Effect of the Invention Since this invention is constituted as explained above, it does an effect as taken below so.
0056 When the signal which produces phase fluctuation (jitter) is inputted into the clock used by a decoder according to the phase synchronization circuit concerning this invention, Since it constitutes so that the response sensitivity of a phase synchronization circuit may be changed to low sensitivity, fluctuation of a phase can be controlled, the abrupt change of a clock signal can be prevented, and it is effective in the ability to perform stable decode operation.
0057 Since the time offset included in a clock is removable according to the phase synchronization circuit concerning this invention, Decoding decoded where it has time offset conventionally turns into decoding at original time, and it is effective in the ability to take an exact synchronization in reproduction of data.

Field of the Invention The digital broadcasting for which this invention uses a broadcasting satellite and a terrestrial wave, the cable TV using a cable. (It is hereafter described as CATV) It is related with the phase synchronization circuit used for the MPEG decoder etc. which restore to the program stream or transport stream compressed by the MPEG standard used with broadcast or DVD.

Description of the Prior Art Drawing 10 is a block diagram of the digital satellite broadcasting receiver which uses the conventional MPEG decoder currently generally used. The input terminal into which 101 inputs an input signal in a figure, the tuner module into which 102 inputs the input signal from the input terminal 1, The descrambler to which 103 considers the output from the tuner module 102 as an input, The MPEG demultiplexer to which 104 considers the output from the descrambler 103 as an input, The MPEG video decoder to which 105 considers the output from the MPEG demultiplexer 104 as an input, The MPEG audio decoders to which 106 considers the output from the MPEG demultiplexer 104 as an input, The NTSC encoder with which 107 considers the output from MPEG video decoder 105 as an input, The output terminal in which 108 outputs an NTSC signal, the D/A converter to which 109 considers the output from MPEG audio decoders as an input, the output terminal in which 110 outputs an analog voice signal, and 111 are CPUs for control.
0003 Explanation of signal processing in a receiver will input first the satellite wave which received with the satellite dish for passing tuner module 102 from the input terminal 101. The tuner module 102 performs decoding of the change of receiving transponders, a recovery, and an error correction, etc., and extracts the MPEG transport stream which the individual data row (stream) multiplexed. It is inputted into the descrambler 103, code release is carried out, and this transport stream (it is hereafter described as TS) is transmitted to the MPEG demultiplexer 104. Program specification information based on a televiewer's channel selection operation in the MPEG demultiplexer 104 (below Program Specific Information:.) PSI -- describing -- it receives, required picture image data and voice data are extracted from TS, and it sends out to MPEG video decoder 105 and MPEG audio decoders 106. MPEG video decoder 105 cancels compression of picture image data, changes it into an NTSC signal with NTSC encoder 107, and outputs an NTSC signal to a television set from the output terminal 108. MPEG audio decoders 106 cancel compression of voice data, change it into an analog voice signal by D/A converter 109, and are outputted to a television set from the output terminal 110. CPU111 for control controls processing of these series.
0004 Also in CATV, the digital signal received via the cable is carried out in the same processing as the above, and is outputted to a television set. Thus, the MPEG demultiplexer 104 has a function which decomposes TS of MPEG contained in the satellite wave which received into picture image data, audio information, and other control data. It also has the function which regenerates the clock signal used with the MPEG demultiplexer 104, MPEG video decoder 105, MPEG audio decoders 106, and NTSC encoder 107 by one side.
0005 The MPEG encoder (coding equipment) which codes and compresses picture image data and voice data by the broadcasting organization side with regeneration of this clock signal, It is time management, i.e., the processing which takes a synchronization, common between the MPEG decoders (decoding device) which cancel compression of picture image data or voice data by the televiewer side. Next, regeneration of a clock signal is explained.
0006 Drawing 11 is a block diagram showing the composition of the phase synchronization circuit used for regeneration of a clock signal. The input terminal into which a TS signal inputs 1 in a figure, the program time reference value included in the TS signal which inputted 2 from the input terminal 1 (below ProgramClock Reference:.) The value of the synchronized signal which is outputted from the counter section 9 mentioned later from describing it as PCR and which serves as a time standard in an MPEG decoder (below System Time Clock:.) STC -- describing -- the subtraction part (phase-comparison part) to subtract and 3 change into an analog signal the digital signal which the subtraction part 2 outputs -- a digital/analog conversion part. (It is hereafter described as a D/A conversion part), the 1st low pass filter to which 4 considers the output of the D/A conversion part 3 as an input. (It is hereafter described as the 1st LPF), the voltage control oscillation part (below Voltage Control Oscillator: describes it as VCO) to which 7 considers the output of 1st LPF4 as an input, the output terminal in which 8 outputs a clock to a latter-part circuit. 9 is a counter section which counts the clock which VCO7 outputs.
0007PCR which was extracted and was separated from TS is used for regeneration of the clock signal in a phase synchronization circuit. In the MPEG decoder in which this PCR contains the video decoder 105 and the audio decoder 106, It is the information for setting up and amending the value of STC to a 27-MHz clock frequency by the case of the value intended by the MPEG encoder side by the side of a broadcast contractor, i.e., MPEG 2, and is contained by a length of 42 bits in the specific stream. If regeneration of the clock signal CLK is explained, the value of PCR first extracted from the specific stream will be written in the counter section 9 as it is (setting up), and STC and PCR which are outputted from the counter section 9 will be initialized as a synchronous state (the same value). The counter 9 makes an initial value written-in PCR, and counts and counts up the receive clock outputted from VCO7. An input of following PCR will perform subtraction treatment with STC from the counter section 9 when PCR is received in the subtraction part 2. When the phase of the clock signal of PCR and STC both is thoroughly in agreement, the output of a subtraction part is set to 0. On the other hand, when both phase is different, the difference is changed into a voltage signal via the D/A conversion part 3 and the 1st LPF4, and it is impressed by VCO7. Phase correction of the CLK is carried out by amending the frequency of the clock signal CLK outputted from VCO7 by this voltage signal. Since the counter section 9 is constituted so that it may count up with the clock signal CLK outputted from VCO7, counted value, i.e., the phase of STC, is controlled according to the output change of VCO7.
0008 Thus, the phase of the clock signal CLK by the side of an MPEG decoder can be correctly coincided the MPEG encoder side by regenerating a clock signal based on PCR. Therefore, the data volume of the buffer memory provided in the video decoder 105 and the audio decoder 106 by being attached overflows, It can prevent that it will be in an underflow state, and the synchronization of the picture image data and voice data using the time-of-day-control information on a reproducing output (below Presentation Time Stamp: describes it as PTS) can be taken. Regeneration of the clock signal by such a phase synchronization circuit is premised on PCR in a stream being generated correctly.

Effect of the Invention Since this invention is constituted as explained above, it does an effect as taken below so.
0056 When the signal which produces phase fluctuation (jitter) is inputted into the clock used by a decoder according to the phase synchronization circuit concerning this invention, Since it constitutes so that the response sensitivity of a phase

synchronization circuit may be changed to low sensitivity, fluctuation of a phase can be controlled, the abrupt change of a clock signal can be prevented, and it is effective in the ability to perform stable decode operation.
0057 Since the time offset included in a clock is removable according to the phase synchronization circuit concerning this invention, Decoding decoded where it has time offset conventionally turns into decoding at original time, and it is effective in the ability to take an exact synchronization in reproduction of data.

Problem to be solved by the invention By the way, the structure of the packet (transport stream packet: it is hereafter described as a TS packet) which carried out time multiplexing of many individual streams, A video elementary stream, the packet elementary stream having contained the audio elementary stream (below Packetized Elementary Stream:.) It has a multiplex layered structure included from PSI, PCR, etc. on the packet described as PES, and a different class from a PES packet.
0010 Therefore, when generating a TS packet directly from the data inputted into the MPEG encoder side, can perform creating and inserting PCR easily, but. If only the data of an elementary stream or a PES packet tends to be compounded and it is going to generate a TS packet, Since PCR is contained on the level of the TS packet, the phase of a clock when elementalist ream is created is not reflected, and it cannot be inserted **can create exact PCR and** .
0011 In order to carry out multiplex and to transmit by other information and time sharing from the relation of a communications network, when the communications network which gathers and transmits access speed is passed, in the transmitting side. Time is read from the counter clocked based on the clock of the reference frequency from the source of a transmitting reference clock at a random interval, and it is transmitted to a communications network as time information PCR.
0012 This time information PCR is read from a counter at intervals of **random** less than 100 ms of predetermined intervals, and that value shows the time T from the last read-out. In a receiver, time information is received as receiving time information via the above-mentioned communications network, and a receive clock is reproduced by the phase synchronization circuit. When a transmission signal gathered and transmits access speed at this time, time compression of the TS data will be carried out to the period shown by the above-mentioned valid data period signal with a valid data period signal, they will be transmitted burstily, a time lag produces them in time information, and the arrival time of receiving time information is changed. Although the above explained TS, The same may be said of the case of a program stream, and it is a system time standard reference value in the case of the above-mentioned program stream (below System Clock Reference:.). SCR -- describing -- it is similarly read from a counter at intervals of **random** less than 700 ms of predetermined intervals, and the value shows the time T from the last read-out. In a receiver, time information is received as receiving time information via the above-mentioned communications network, and a receive clock is reproduced by the phase synchronization circuit.
0013 Change of the above arrival time of time information appeared as fluctuation of the phase of STC (jitter), and since fluctuation of this kind of phase could not be controlled, the transmission signal in the above communications networks had the problem that stable receiving operation could not be performed in the conventional phase synchronization circuit.
0014 Although the buffer of the received data is carried out to dissolution of the above problems and the method of transmitting at a fixed rate approximately from a buffer using the transmission rate shown in the syntax of received data is indicated in ITUT-T advice H.220.0, Since the above-mentioned transmission rate did not necessarily show the exact rate, it had the problem that the sufficiency degree of the data in a buffer had to be supervised and controlled in addition to adding a buffer.
0015 By reproducing a clock with accuracy sufficient even when it was made in order that this invention might cancel above SUBJECT, and fluctuation of a phase occurs near the sampling frequency, While being able to prevent the data volume of the buffer memory provided in the video decoder 105 and the audio decoder 106 by being attached from being in overflow and an underflow state, It aims at providing the phase synchronization circuit which can take the synchronization of the picture image data and voice data using PTS of the reproducing output.

Means for solving problem The phase synchronization circuit which this invention requires for this invention is characterized by that the phase synchronization circuit which performs synchronous processing of said clock signal based on the difference value of the phase of the clock signal used by the decoder side and the phase of the base period information included in an input signal comprises:
The judging means which judges whether said input signal is a signal which makes the phase of said clock signal produce fluctuation.
The alteration means which changes the response sensitivity of synchronous processing based on the decided result of said judging means.

0017 The phase synchronization circuit concerning this invention was constituted so that it might make response sensitivity of synchronous processing lower than a specified value, in being a signal with which said input signal makes the phase of said clock signal produce fluctuation for said alteration means.
0018 When the period when the phase synchronization circuit concerning this invention becomes larger than a threshold value with the absolute value of said difference value about said judging means continues more than a prescribed period, Or when the probability which becomes larger than a threshold value with said absolute value became beyond a specified value, it constituted so that it might judge with said input signal being a signal which makes the phase of said clock signal produce fluctuation.
0019 The absolute value calculation part in which the phase synchronization circuit concerning this invention computes the absolute value of said difference value for said judging means, The updown counter which carries out down counting of the computed difference absolute value as compared with the 1st threshold value in being larger than the 1st threshold value, and being small, a rise count and, The counted value of said updown counter is judged as said input signal being a signal which makes the phase of said clock signal produce fluctuation as compared with the 2nd threshold value, when larger than the 2nd threshold value, When small, said input signal consisted of comparators judge that are not the signals which make the phase of said clock signal produce fluctuation.

0020 The absolute value calculation part in which the phase synchronization circuit concerning this invention computes the absolute value of said difference value for said judging means, According to the size of the output of the smooth sections which predetermined-number-collection-********** the computed difference absolute value, and said smooth sections, said input signal judged the grade which makes the phase of said clock signal produce fluctuation, and consisted of control signal generating sections which generate the control signal according to a decided result.
0021 The phase synchronization circuit concerning this invention considers as an input the data which expresses effective and the invalidity of an input signal for said judging means, When the period when invalid data is inputted continued more than a prescribed period, or when the probability that invalid data will be inputted became beyond a specified value, it constituted so that it might judge with said input signal being a signal which makes the phase of said clock signal produce fluctuation.
0022 The phase synchronization circuit concerning this invention considers as an input the data which expresses effective and the invalidity of an input signal for said judging means, The updown counter which carries out down counting in being small, a rise count and whenever it asks for the period which invalid data inputs, and invalid data inputs the period for which it asked, in being larger than the 1st threshold value as compared with the 1st threshold value, The counted value of said updown counter is judged as said input signal being a signal which makes the phase of said clock signal produce fluctuation as compared with the 2nd threshold value, when larger than the 2nd threshold value, When small, said input signal consisted of comparators judge that are not the signals which make the phase of said clock signal produce fluctuation.
0023 The smooth sections which predetermined-number-collection-********** the period which the phase synchronization circuit concerning this invention considers as an input the data which expresses effective and the invalidity of an input signal for said judging means, and invalid data inputs, According to the size of the output of said smooth sections, said input signal judged the grade which makes the phase of said clock signal produce fluctuation, and consisted of control signal generating sections which output the control signal according to a decided result.
0024 The phase synchronization circuit concerning this invention was constituted so that a change of the response sensitivity in said alteration means might be made by change of the pass band of the low pass filter used for synchronous processing.
0025 The phase synchronization circuit concerning this invention was constituted so that a change of the response sensitivity in said alteration means might be made by change of the multiplication coefficient of the coefficient unit used for synchronous processing.
0026 The smooth sections which predetermined-number-collection-********** the period which the phase synchronization circuit concerning this invention considers the data showing effective and the invalidity of an input signal as an input, and invalid data inputs, It constituted so that it might have further the amount calculation part of time gaps which computes the amount of time gaps of said clock signal based on the output of said smooth sections, and a compensation means which said clock signal amends based on the computed amount of time gaps.
0027
Mode for carrying out the invention Hereafter, this invention is concretely explained based on Drawings in which that embodiment is shown.
Embodiment 1. drawing 1 shows a phase synchronization circuit of an MPEG data receiver which is this embodiment of the invention 1. An input terminal into which PCR contained in a TS signal inputs 1 in the figure, A subtraction part which subtracts STC outputted from the counter section 9 mentioned later from PCR which 2 inputted, A D/A conversion part which changes into an analog signal a digital signal value to which the subtraction part 2 outputs 3, The 1st LPF to which 4 considers an output of the D/A conversion part 3 as an input, the 2nd LPF to which five consider an output of the D/A conversion part 3 as an input, 6 is a switch part which changes and outputs an output of 1st LPF4, and an output of 2nd LPF5 based on an output of the comparator 17 mentioned later, and response sensitivity of a phase synchronization circuit is changed by this switch part. VCO to which 7 considers an output of the switch part 6 as an input, an output terminal which outputs a receive clock which outputs eight from VCO, A counter section which counts a receive clock which outputs 9 from VCO, an output terminal which outputs STC which outputs 10 from the counter section 9 to the latter part, An absolute value calculation part which considers a digital signal value which outputs 11 from the subtractor 2 as an input, A threshold value 12 indicates any value to be, a comparator to which 13 considers an output and the threshold value 12 of the absolute value calculation part 11 as an input, An initial value of the updown counter 15 which 14 mentions later, an updown counter to which 15 considers an output and the initial value 14 of the comparator 13 as an input, a threshold value 16 indicates any value to be, and 17 are comparators which consider an output and the threshold value 16 of the updown counter 15 as an input. The absolute value calculation part 11 thru/or the comparator 17 constitute a judging means.
0028 The subtraction part 2 performs subtraction treatment of PCR inputted from the input terminal 1, and STC outputted from the counter section 9. When the phase of the clock signal of PCR and STC both is thoroughly in agreement, the output of the subtraction part 2 is set to 0. On the other hand, when both phase is different, the difference value outputs to the D/A conversion part 3 and the absolute value calculation part 11. The 1st LPF4 that differed in the characteristic changed by the switch part 6 by the decision signal from a judging means, and the 2nd LPF5 are in the output of the D/A conversion part 3, it is worn, is changed into a voltage signal via ** one side, and is impressed to VCO7. By amending the frequency of a receive clock with said voltage signal, VCO7 amends a phase and it outputs it to the output terminal 8. Since the counter section 9 is constituted so that the receive clock outputted from VCO7 may be counted up, counted value, i.e., the phase of STC, is controlled according to the output change of VCO7.
0029 The absolute value calculation part 11 computes the absolute value of the difference value outputted from the subtraction part 2, when the absolute value of this difference value is larger than the arbitrary threshold values 12 with the comparator 13, whenever PCR comes, it makes the updown counter 15 count up, and when small, it is made to count down. The comparator 17 changes the switch part 6 so that a voltage signal may pass the 1st LPF4 **same** as a conventional example, when the counted value of the updown counter 15 is smaller than the arbitrary threshold values 16, The switch part 6 is changed so that a voltage signal may pass the 2nd LPF5 that passes only a lower zone compared with the 1st LPF4, in being large. The updown counter 15 shall initialize an initial value, whenever new TS is inputted and a phase synchronization circuit starts synchronous processing.
0030A time lag arises at the arrival time of PCR by time compression of the TS data being carried out by transmission signal processing etc., and transmitting them burstily by the above operation, If the value of the counter 15 of an updown counter will become large if the probability that the absolute value of the difference value of above-mentioned PCR and STC of an MPEG decoder will be computed more greatly than the arbitrary threshold values 12 increases, and this value becomes larger than the arbitrary threshold values 16, A judging means judges with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, and changes LPF which is a loop filter of a phase synchronization circuit to the 2nd LPF5 that is low sensitivity. Thereby, a phase synchronization circuit performs synchronous processing which carries out a low sensitivity

response, and can control fluctuation of a phase.

0031 Embodiment 2. drawing 2 shows the phase synchronization circuit of the MPEG data receiver which is this embodiment of the invention 2. The input terminal which inputs the valid data period signal which shows the period when valid data is inputted in the figure among the TS signals which 18 inputs, The counter section which considers as an input the valid data period signal which inputs 19 from the input terminal 18, The threshold value 20 indicates any value to be, the comparator to which 21 considers the output and the threshold value 20 of the counter section 19 as an input, The threshold value 22 indicates any value to be, the initial value of the updown counter 23 which 22 mentions later, the updown counter to which 23 considers the output and the initial value 22 of the comparator 21 as an input, the threshold value 24 indicates arbitration to be, and 25 are comparators which consider the output and the threshold value 24 of the updown counter 23 as an input. A judging means is constituted by the counter section 19 thru/or the comparator 25.

0032 The counter section 19 counts with a receive clock with the time as the starting point of the input start of the invalid data being carried out using the valid data period signal which shows the period when valid data is inputted among the TS signals inputted from the input terminal 18, and evaluates invalid period width as counted value of a receive clock. When the evaluated invalid period width has the large invalid period width which was compared with the threshold values 20 with an arbitrary twist, and was evaluated by the comparator 21, whenever invalid data is inputted, the updown counter 23 is made to count up, and it is made to count down when small. The comparator 25 changes the switch part 6 so that a voltage signal may pass the 1st LPF4 **same** as a conventional example, when the counted value of the updown counter 23 is smaller than the arbitrary threshold values 24, The switch part 6 is changed so that a voltage signal may pass the 2nd LPF5 that passes only a lower zone compared with the 1st LPF4, in being large. The updown counter 23 shall initialize an initial value, whenever TS is inputted and a phase synchronization circuit starts synchronous processing.

0033 When a signal which a time lag produces at the arrival time of PCR by time compression of the TS data being carried out by the above operation, and transmitting them burstily by it is inputted, If the frequency which comes using the valid data period signal which shows the period when valid data is inputted among TS signals by width with larger invalid period width than the arbitrary threshold values 20 becomes high, counter 23 value of an updown counter will become large, If this value becomes larger than the arbitrary threshold values 24, a judging means will judge with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, and will change LPF which is a loop filter of a phase synchronization circuit to the 2nd LPF5 that is low sensitivity. Thereby, a phase synchronization circuit performs synchronous processing which carries out a low sensitivity response, and can control fluctuation of a phase.

0034 Embodiment 3. drawing 3 shows the phase synchronization circuit of the MPEG data receiver which is this embodiment of the invention 3. The 1st coefficient unit with which 26 considers the output of the subtractor 2 as an input in the figure, the 2nd coefficient unit with which 27 considers the output of the subtractor 2 as an input, 28 is a selector which changes the output of the 1st coefficient unit 26, and the output of the 2nd coefficient unit 27 based on the output of the comparator 17, and the response sensitivity of a phase synchronization circuit is changed by this selector. The adding machine with which 29 considers the output of the selector 28 and the output of a D flip-flop mentioned later as an input, and 30 are D flip-flops which consider the output of the adding machine 29 as an input. About a judging means, it is the same as that of what was explained by Embodiment 1.

0035 The 1st coefficient unit 26 carries out the multiplication of the coefficient A of $0< A<1$ to the difference value of the subtractor 2, and the 2nd coefficient unit 27 carries out the multiplication of the coefficient B of $0<B<A<1$. The selector 28 chooses the difference value by which multiplication was carried out with the 1st coefficient unit, when the counted value of the updown counter 15 is smaller than the arbitrary threshold values 16, and when large, it chooses the difference value by which multiplication was carried out with the 2nd coefficient unit. The adding machine 29 adds the difference value by which multiplication was carried out by one of coefficients, and the digital value of the control voltage outputted from D flip-flop 30 mentioned later. D flip-flop 30 is memorized to timing each time the digital value of the control voltage outputted from the adding machine 29 is inputted into PCR. The D/A conversion part 3 changes into a voltage signal the value memorized by the D flip-flop, and impresses it to VCO7.

0036A time lag arises at the arrival time of PCR by time compression of the TS data being carried out by the above operation, and transmitting them burstily by it, If the probability that the absolute value of a difference value with STC which is a value of the synchronized signal used as above-mentioned PCR and the time standard of an MPEG decoder will be computed more greatly than the arbitrary threshold values 12 increases, the value of the counter 15 of an updown counter will become large, When this value becomes larger than the arbitrary threshold values 16, a judging means, It judges with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, and the 1st coefficient unit 26 of a phase synchronization circuit, the adding machine 29, and the coefficient unit of the digital gone type loop filter constituted from D flip-flop 30 are changed to the 2nd coefficient unit that carries out multiplication by a smaller coefficient. Thereby, a phase synchronization circuit performs synchronous processing which carries out a low sensitivity response, and can control fluctuation of a phase.

0037 Embodiment 4. drawing 4 shows the phase synchronization circuit of the MPEG data receiver which is this embodiment of the invention 4. In the figure, 28 is a selector which changes the output of the 1st coefficient unit 26, and the output of the 2nd coefficient unit 27 based on the output of the comparator 25, and the response sensitivity of a phase synchronization circuit is changed by this selector. The judging means is the same as that of Embodiment 2.

0038 The selector 28 chooses the difference value by which multiplication was carried out with the 1st coefficient unit, when the counted value of the updown counter 23 is smaller than the arbitrary threshold values 24, and when large, it chooses the difference value by which multiplication was carried out with the 2nd coefficient unit.

0039 When a signal which a time lag produces at the arrival time of PCR by time compression of the TS data being carried out by the above operation, and transmitting them burstily by it is inputted, If the frequency which comes using the valid data period signal which shows the period when valid data is inputted among TS signals by width with larger invalid period width than the arbitrary threshold values 20 becomes high, counter 23 value of an updown counter will become large, If this value becomes larger than the arbitrary threshold values 24, a judging means will judge with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, The 1st coefficient unit 26 of a phase synchronization circuit, the adding machine 29, and the coefficient unit of the digital gone type loop filter constituted from D flip-flop 30 are changed to the 2nd coefficient unit that carries out multiplication by a smaller coefficient. Thereby, a phase synchronization circuit performs synchronous processing which carries out a low sensitivity response, and can control fluctuation of a phase.

0040 Embodiment 5. drawing 5 shows the phase synchronization circuit of the MPEG data receiver which is this embodiment of the invention 5. The smooth sections to which 31 considers the output of the absolute value calculation part 11 as an input in the figure, The control signal generating section to which 32 considers the output of the smooth sections 31 as an input,

and 33 are coefficient-of-variable-capacitance machines which change the coefficient which carries out multiplication to the output of the subtractor 2 based on the output of the control signal generating section 32, and the response sensitivity of a phase synchronization circuit is changed with this coefficient-of-variable-capacitance machine. 29 is an adding machine adding the output and D flip-flop 30 of the coefficient-of-variable-capacitance machine 33. The absolute value calculation part 11, the smooth sections 31, and the control signal generating section 32 constitute a judging means.

0041 The coefficient-of-variable-capacitance machine 33 carries out the multiplication of the coefficient X of 0< X<1 to the difference value of the subtractor 2. The coefficient X is gradually changed by the control signal outputted from the control signal generating section 32 mentioned later. The adding machine 29 adds the difference value by which multiplication was carried out with the coefficient-of-variable-capacitance machine, and the digital value of the control voltage outputted from D flip-flop 30 mentioned later. D flip-flop 30 is memorized to timing each time the digital value of the control voltage outputted from the adding machine 29 is inputted into PCR. The D/A conversion part 3 changes into a voltage signal the value memorized by D flip-flop 30, and impresses it to VCO7.

0042 The absolute value calculation part 11 computes the absolute value of the difference value outputted from said subtraction part 2, and carries out smoothness of the absolute value of the difference value in which number-of-times calculation of arbitrary was carried out by the smooth sections 31. The control signal generating section 32 generates the control signal according to the value outputted from the smooth sections 31. The coefficient-of-variable-capacitance machine 33 changes a coefficient gradually so that the value outputted from the smooth sections 31 is large, and the coefficient X may become small.

0043A time lag arises at the arrival time of PCR by time compression of the TS data being carried out by the above operation, and transmitting them burstily by it, A difference value with STC which is a value of the synchronized signal used as above-mentioned PCR and the time standard of an MPEG decoder is computed, If smoothness of the absolute value of the difference value is carried out by a part for the number of times of arbitrary and the value becomes large, a judging means will judge with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, It is made to carry out the multiplication of the coefficient which changed gradually the coefficient of the digital gone type loop filter constituted from the multistage coefficient unit 33, the adding machine 29, and D flip-flop 30 of a phase synchronization circuit, and changed it according to the value. Thereby, warm synchronous processing can be performed and fluctuation of a phase is controlled rather than a phase synchronization circuit carries out the low sensitivity response according to the state of the TS data inputted. A phase synchronization circuit may be constituted like Embodiment 1, and although the case where the multiplication coefficient of the coefficient-of-variable-capacitance machine 33 was changed based on the output of the control signal generating section 32 was explained, it may constitute from this embodiment so that switching control of the pass band of LPF may be carried out.

0044 Embodiment 6. drawing 6 shows the phase synchronization circuit of the MPEG data receiver which is this embodiment of the invention 6. The smooth sections to which 34 considers the output of the counter section 19 as an input in the figure, the control signal generating section to which 35 considers the output of the smooth sections 34 as an input, 33 is a coefficient-of-variable-capacitance machine which changes the coefficient which carries out multiplication to the output of the subtractor 2 based on the output of the control signal generating section 35, and the response sensitivity of a phase synchronization circuit is changed with this coefficient-of-variable-capacitance machine. The counter section 19, the smooth sections 34, and the control signal generating section 35 constitute a judging means.

0045 The smooth sections 34, Smoothness of the invalid period width counted and evaluated with the receive clock with the time as the starting point of the input start of the invalid data being carried out using the valid data period signal which shows the period when valid data is inputted among the TS signals counted by the counter section 19 is carried out by a part for the number of times of arbitrary at which invalid data arrived. The control signal generating section 35 generates a control signal according to the value outputted from the smooth sections 34. The coefficient-of-variable-capacitance machine 33 changes a coefficient gradually so that the value outputted from the smooth sections 35 is large, and the coefficient X may become small.

0046 When a signal which a time lag produces at the arrival time of PCR by time compression of the TS data being carried out by the above operation, and transmitting them burstily by it is inputted, Invalid period width is predetermined-number-collection-********(ed) using the valid data period signal which shows the period when valid data is inputted among TS signals. And if the value becomes large, a judging means will judge with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, The multiplication of the coefficient which changed gradually the coefficient of the digital gone type loop filter constituted from the coefficient-of-variable-capacitance machine 33, the adding machine 29, and D flip-flop 30 of a phase synchronization circuit, and changed it according to the value is carried out. rather than a phase synchronization circuit carries out the low sensitivity response according to the state of the TS data inputted by this -- texture -- warm synchronous processing can be performed and fluctuation of a phase can be controlled. A phase synchronization circuit may be constituted like Embodiment 2, and although the case where the multiplication coefficient of the coefficient-of-variable-capacitance machine 33 was changed based on the output of the control signal generating section 35 was explained, it may constitute from this embodiment so that switching control of the pass band of LPF may be carried out.

0047 Embodiment 7. drawing 7 shows the phase synchronization circuit of the MPEG data receiver which is this embodiment of the invention 7. The smooth sections to which 34 considers the output of the counter section 19 as an input in the figure, the amount calculation part of time gaps to which 36 considers the output of the smooth sections 34 as an input, The adding machine with which 37 considers the output of STC which is an output from the counter section 9, and the amount calculation part 36 of time gaps as an input, and 10 are output terminals which output amended STC which is outputted from the adding machine 37 to the latter part. Since the composition of those other than smooth-sections 34, amount calculation part 36 of time gaps, and adding machine 37 is the same as that of Embodiment 2, detailed explanation is omitted.

0048 The smooth sections 34, Smoothness of the invalid period width counted and evaluated with the receive clock with the time as the starting point of the input start of the invalid data being carried out using the valid data period signal which shows the period when valid data is inputted among the TS signals counted by the counter section 19 is carried out by a part for the number of times of arbitrary at which invalid data arrived. The amount calculation part 36 of time gaps computes the time lag of the arrival time of PCR produced by time compression of the TS data being carried out, and being burstily transmitted from the evaluated invalid period width which is outputted from the smooth sections 34, converts this time lag into the counted value of a receive clock, and outputs it. The adding machine 37 functions as a compensation means which adds STC outputted from the counter 9, and the time lag converted into the counted value of the receive clock outputted from the amount calculation part 36 of time gaps, and outputs it to the latter part as an amended STC.

0049 When a signal which a time lag produces at the arrival time of PCR by time compression of the TS data being carried

out by the above operation, and transmitting them burstily by it is inputted, If the frequency which comes using the valid data period signal which shows the period when valid data is inputted among TS signals by width with larger invalid period width than the fixed threshold value 20 becomes high, counter 23 value of an updown counter will become large, If this value becomes larger than the arbitrary threshold values 24, a judging means will judge with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, and will change LPF which is a loop filter of a phase synchronization circuit to the 2nd LPF5 that is low sensitivity. Smoothness of the invalid period width is carried out by a part for the number of times of arbitrary at which invalid data arrived (smooth sections 34), the amount of time gaps of STC which made it generate by a phase synchronization circuit based on this value is computed (the amount calculation part 36 of time gaps), and correction value is added in the adding machine 37. A time gap of STC which performed synchronous processing which carries out a response **low sensitivity phase synchronization circuit** by these operations, and could control fluctuation of a phase, and was generated in the phase synchronization circuit can be amended and MPEG-decoded.

0050 Embodiment 8. drawing 8 shows the phase synchronization circuit of the MPEG data receiver which is this embodiment of the invention 8. The composition except the smooth sections 34, the amount calculation part 36 of time gaps, and the adding machine 37 is the same as that of drawing 4 explained in Embodiment 4 so that clearly from a figure.

0051 It is the same and operation is explained briefly hereafter as Embodiments 4 and 7 mentioned above explained. When a signal which a time lag produces by carrying out time compression of the TS data, and transmitting them burstily at the arrival time of PCR is inputted, If the frequency which comes using the valid data period signal which shows the period when valid data is inputted among TS signals by width with larger invalid period width than the arbitrary threshold values 20 becomes high, counter 23 value of an updown counter will become large, If this value becomes larger than the arbitrary threshold values 24, a judging means will judge with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, The 1st coefficient unit 26 of a phase synchronization circuit, the adding machine 29, and the coefficient unit of the digital gone type loop filter constituted from D flip-flop 30 are changed to the 2nd coefficient unit that carries out multiplication by a smaller coefficient. Smoothness of the invalid period width is carried out by a part for the number of times of arbitrary at which invalid data arrived, the amount of time gaps of STC which made it generate by a phase synchronization circuit based on this value is computed, and this correction value is added in the adding machine 37. While performing synchronous processing which carries out a response **low sensitivity phase synchronization circuit** by these operations and being able to control fluctuation of a phase, a time gap of STC generated in the phase synchronization circuit can be amended and MPEG-decoded.

0052 Embodiment 9. drawing 9 shows the phase synchronization circuit of the MPEG data receiver which is this embodiment of the invention 9. The composition except the amount calculation part 36 of time gaps and the adding machine 37 is the same as that of drawing 6 explained in Embodiment 6 so that clearly from a figure.

0053 It is the same and operation is explained briefly hereafter as Embodiments 6 and 7 mentioned above explained. When a signal which a time lag produces by carrying out time compression of the TS data, and transmitting them burstily at the arrival time of PCR is inputted, invalid period width is predetermined-number-collection-********(ed) using the valid data period signal which shows the period when valid data is inputted among TS data. And if the value becomes large, a judging means will judge with the TS data which produce the fluctuation of the phase of STC (jitter) being inputted, Multiplication is carried out by the calculation which changed gradually the coefficient of the digital gone type loop filter constituted from the multistage coefficient unit 33, the adding machine 29, and D flip-flop 30 of a phase synchronization circuit, and changed it according to the value. Smoothness of the invalid period width is carried out by a part for the number of times of arbitrary at which invalid data arrived, the amount of time gaps of STC generated by the phase synchronization circuit based on this value is computed, and that correction value is added in the adding machine 37. A time gap of STC which performed synchronous processing which carries out the low sensitivity response according to the state of TS data where a phase synchronization circuit is inputted by these operations, and could control fluctuation of a phase, and was generated in the phase synchronization circuit can be amended and MPEG-decoded.

0054 Although Embodiments 1-9 explain by extracting and processing PCR contained in the TS signal by setting an input signal to TS, an effect also with same also extracting and processing SCR contained in a program stream by making an input signal into a program stream is acquired. Although the above-mentioned Embodiments 7-9 explained what provided the circuit for STC amendment (the smooth sections 34, the amount calculation part of time gaps, the adding machine 37) to the phase synchronization circuit of Embodiments 2, 4, and 6, naturally it may be made to provide to the phase synchronization circuit of Embodiments 1, 3, and 5. For example in the phase synchronization circuit of drawing 1, drawing 3, and drawing 5, namely, the valid data period signal input terminal 18, the counter section 19, the smooth sections 34, the amount calculation part of time gaps, It connects so that the adding machine 37 may be added, the output of VCO7 may be made to input also into the counter 19 and the adding machine 37 may be made to be placed between from the subtractor 2 before the output terminal 10.

Brief Description of the Drawings

Drawing 1 It is a phase simulation circuit diagram showing this embodiment of the invention 1.
Drawing 2 It is a phase simulation circuit diagram showing this embodiment of the invention 2.
Drawing 3 It is a phase simulation circuit diagram showing this embodiment of the invention 3.
Drawing 4 It is a phase simulation circuit diagram showing this embodiment of the invention 4.
Drawing 5 It is a phase simulation circuit diagram showing this embodiment of the invention 5.
Drawing 6 It is a phase simulation circuit diagram showing this embodiment of the invention 6.
Drawing 7 It is a phase simulation circuit diagram showing this embodiment of the invention 7.
Drawing 8 It is a phase simulation circuit diagram showing this embodiment of the invention 8.
Drawing 9 It is a phase simulation circuit diagram showing this embodiment of the invention 9.
Drawing 10 It is a figure showing the digital satellite broadcasting receiver which uses the conventional MPEG decoder.
Drawing 11 It is the conventional phase simulation circuit diagram.

Explanations of letters or numerals

1 An input terminal and 2 A subtractor, 3 digital/analog converters, and 4 The 1st low pass filter, 5 The 2nd low pass filter and 6 A switch and 7 Voltage control oscillation part, 8 An output terminal, 9 counter sections, and 10 An output terminal, 11 absolute-value calculation part, Twelve threshold values and 13 A comparator and 14 An initial value, 15 updown counters, 16 threshold values and 17 A comparator and 18 An input terminal, 19 counter sections, and 20 Threshold value, 21

comparators and 22 An initial value and 23 An updown counter and 24 Threshold value, 25 A comparator and 26 The 1st coefficient unit and 27 The 2nd coefficient unit and 28 Selector, 29 An adding machine, 30 D flip-flops, and 31 Smooth sections and 32 Control signal generating section, 33 coefficient-of-variable-capacitance machine and 34 Smooth sections and 35 A control signal generating section and 36 The amount calculation part of time gaps, 37 An adding machine and 101 An input terminal and 102 Tuner module, 103 A descrambler, a 104 MPEG demultiplexer, 105 MPEG video decoders, 106 MPEG audio decoders, 107 NTSC encoders, and 108 An output terminal, 109 D/A converters, and 110 An output terminal and 111 CPU for control.

Drawing 1

For drawings please refer to the original document.

Drawing 2

For drawings please refer to the original document.

Drawing 3

For drawings please refer to the original document.

Drawing 4

For drawings please refer to the original document.

Drawing 5

For drawings please refer to the original document.

Drawing 6

For drawings please refer to the original document.

Drawing 7

For drawings please refer to the original document.

Drawing 10

For drawings please refer to the original document.

Drawing 8

For drawings please refer to the original document.

Drawing 9

For drawings please refer to the original document.

Drawing 11

For drawings please refer to the original document.

For drawings please refer to the original document.